P3P622S01J

Timing-Safe™ Peak EMI Reduction IC

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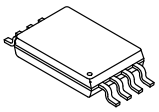


TSSOP8 4.4x3
CASE 948AL

Functional Description

P3P622S01J is a versatile, 3.3 V Zero−delay buffer designed to distribute low frequency Timing−Safe Clocks with Peak EMI Reduction.

P3P622S01J accepts an input clock either from a fundamental Crystal or from an external reference clock.

P3P622S01J accepts one reference input and drives out two low−skew clocks.

P3P622S01J has an on−chip PLL that locks to an input reference clock. The PLL feedback is on−chip and is obtained from the CLKOUT pad, internal to the device.

Multiple P3P622S01J devices can accept the same input clock and distribute it. In this case, the skew between the outputs of the two devices is guaranteed to be less than 700 pS.

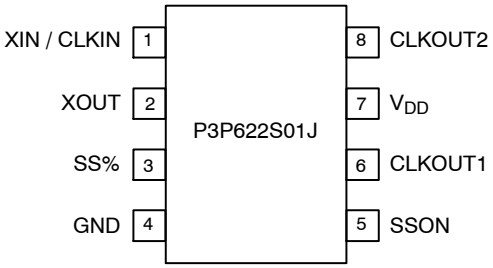
The output has less than 200 pS of cycle−to−cycle jitter. The input and output propagation delay is guaranteed to be less than 250 pS, and the output−to−output skew is guaranteed to be less than 250 pS.

Refer “Spread Spectrum Control and Input−Output Skew Table” for deviations and Input−Output Skew.

General Features

- Low Frequency Clock Distribution with Timing−Safe Peak EMI Reduction
- Input Frequency Range: 4 MHz − 20 MHz
- Zero Input − Output Propagation Delay
- Low−skew Outputs:
  - Output−output Skew Less than 250 pS
  - Device−device Skew Less than 700 pS
- Less than 200 pS Cycle−to−cycle Jitter
- Available in 8 Pin, 4.4 mm TSSOP Package
- Supply Voltage: 3.3 V ± 0.3 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Spread Spectrum Frequency Generation

The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi−layer PCBs etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency.P3P622S01J uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation.

Timing−Safe Technology

Timing−Safe technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

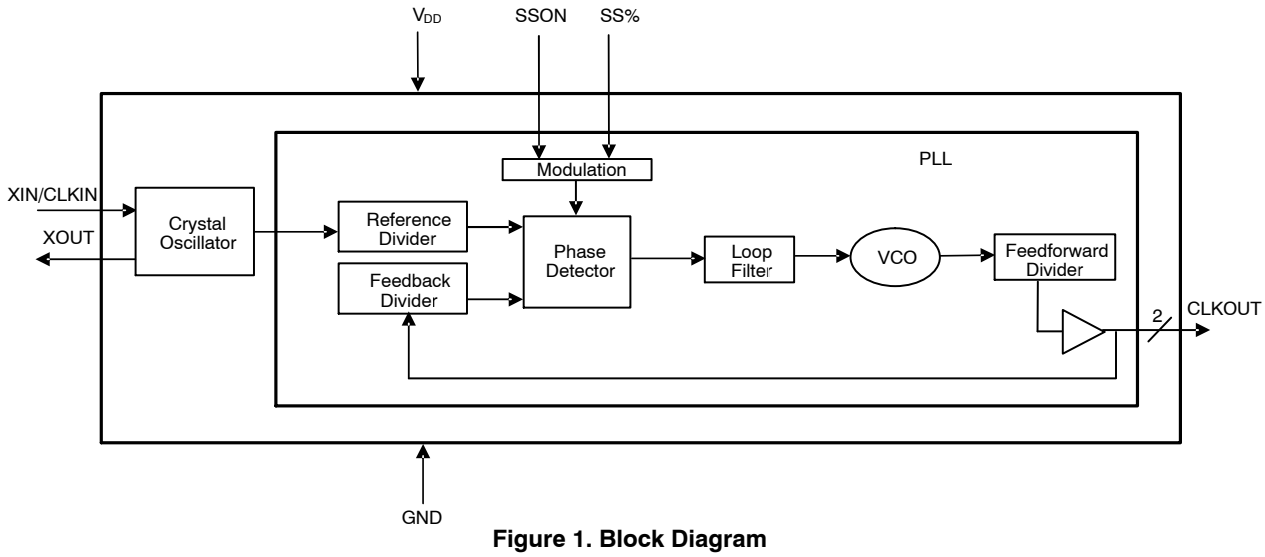


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION FOR P3P622S01J

Pin #	Pin Name	Description
1	XIN / CLKIN	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
2	XOUT	Crystal connection. If using an external reference, this pin must be left unconnected.
3	SS% (Note 2)	Spread Spectrum Selection
4	GND	Ground.
5	SSON (Note 2)	Spread Spectrum enable and disable option When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum.
6	CLKOUT1 (Note 1)	Buffered clock output
7	V_{DD}	3.3 V supply
8	CLKOUT2 (Note 1)	Buffered clock output

1. Weak pull−down on all outputs. Buffered clock outputs are Timing−Safe
2. Weak pull−up on these inputs.

Table 2. SPREAD SPECTRUM CONTROL AND INPUT−OUTPUT SKEW TABLE

Device	Input Frequency	SS%	Deviation	Input−Output Skew ($\pm T_{SKEW}$)
P3P622S01J	12 MHz	0	±0.25%	0.063
		1	±0.50%	0.125

NOTE: T_{SKEW} is measured in units of the Clock Period

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD	Voltage on any input pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. OPERATING CONDITIONS

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	−40	+85	°C
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Table 5. ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Units
V_{IL}	Input LOW Voltage (Note 1)				0.8	V
V_{IH}	Input HIGH Voltage (Note 1)		2.0			V
I_{IL}	Input LOW Current	V_{IN} = 0 V			50	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}			100	μA
V_{OL}	Output LOW Voltage (Note 2)	I_{OL} = 8 mA			0.4	V
V_{OH}	Output HIGH Voltage (Note 2)	I_{OH} = −8 mA	2.4			V
I_{DD}	Supply Current	Unloaded outputs		15		mA
Z_O	Output Impedance			23		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

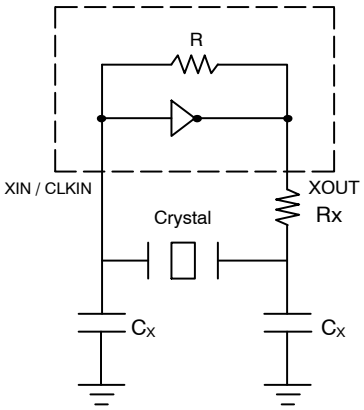
1. CLKIN input has a threshold voltage of VDD/2
2. Parameter is guaranteed by design and characterization. Not tested in production.

Table 6. SWITCHING CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Units
	Input Frequency		4		20	MHz
$1/t_1$	Output Frequency	30 pF load	4		20	MHz
t_D	Duty Cycle (Note 4) = (t_2/t_1) * 100	Measured at $V_{DD}/2$	40	50	60	%
t_3	Output Rise Time (Notes 3 and 4)	Measured between 0.8 V and 2.0 V			2.5	nS
t_4	Output Fall Time (Notes 3 and 4)	Measured between 2.0 V and 0.8 V			2.5	nS
t_5	Output−to−output skew (Note 4)	All outputs equally loaded			250	pS
t_6	Delay, CLKIN Rising Edge to CLKOUT Rising Edge (Note 4)	Measured at $V_{DD}/2$			±250	pS
t_7	Device−to−Device Skew (Note 4)	Measured at $V_{DD}/2$ on the CLKOUT pins of the device			700	pS
t_J	Cycle−to−cycle jitter (Note 4)	Loaded outputs			200	pS
t_{LOCK}	PLL Lock Time (Note 4)	Stable power supply, valid clock presented on CLKIN pin			1.0	mS

3. The parameters specified with loaded outputs.
4. Parameter is guaranteed by design and characterization. Not tested in production.

Typical Crystal Interface Circuit



$C_X = 2*(C_P - C_S)$,
Where C_P = Load capacitance of crystal specified in a Crystal Datasheet
C_S = Stray capacitance due to C_{IN}, PCB, Trace, etc.
C_X = Load capacitance to be used
Rx is used to reduce power dissipation in the Crystal

Figure 2. Typical Crystal Interface Circuit

Switching Waveforms

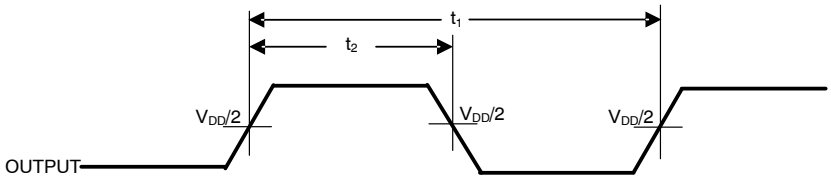


Figure 3. Duty Cycle Timing

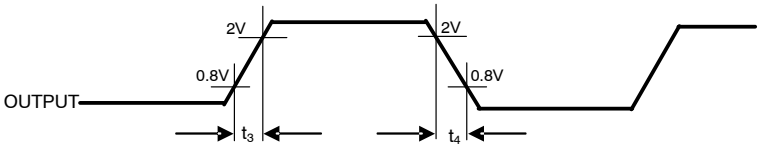


Figure 4. All Outputs Rise/Fall Time

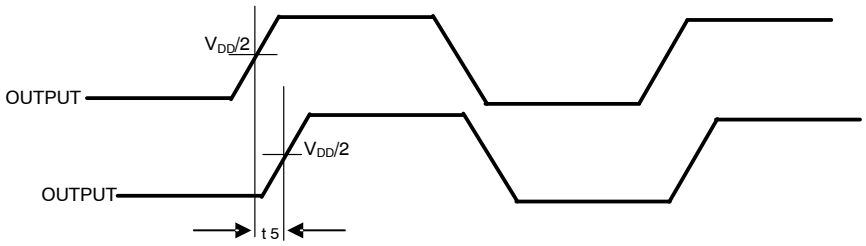


Figure 5. Output−Output Skew

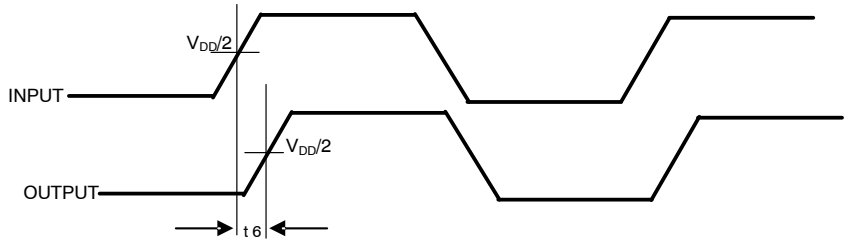


Figure 6. Input−Output Propagation Delay

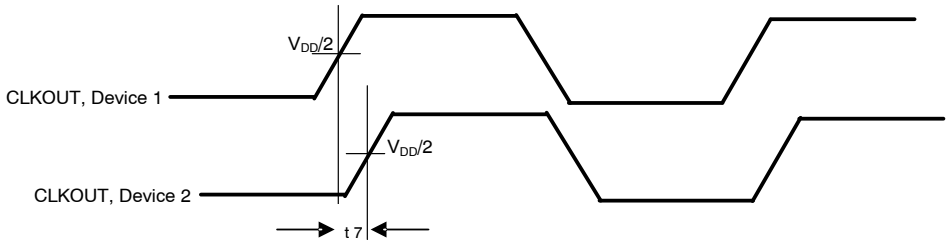


Figure 7. Device−Device Skew

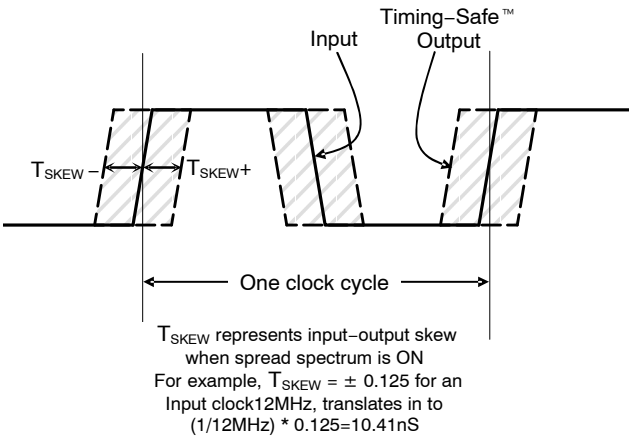


Figure 8. Input−Output Skew

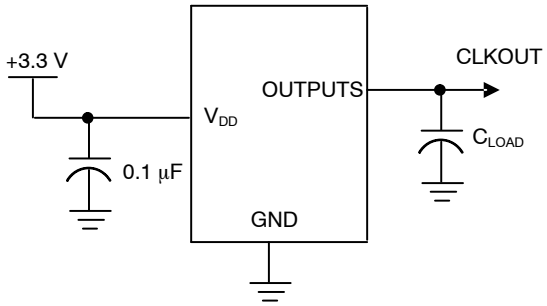


Figure 9. Test Circuit

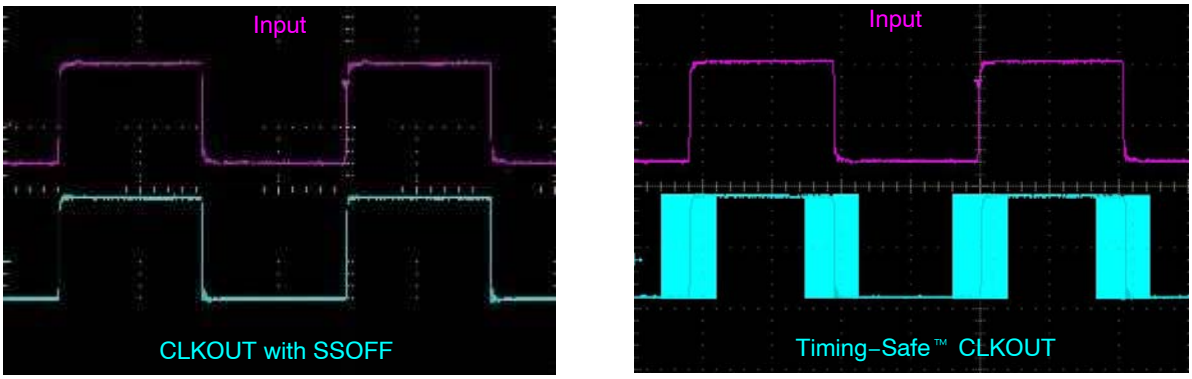


Figure 10. A Typical Example of Timing−Safe Waveform

Table 7. ORDERING INFORMATION

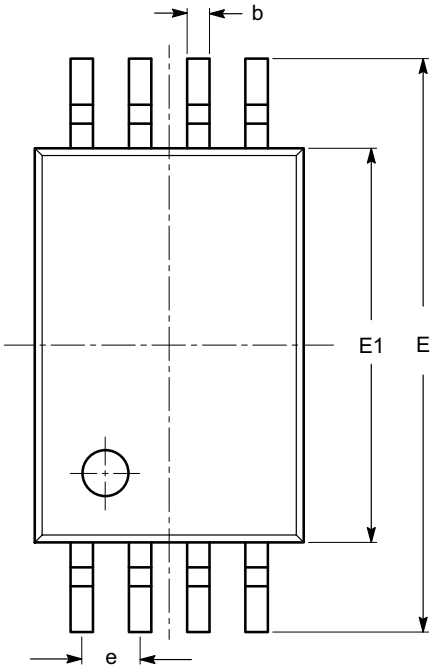
Part Number	Marking	Package Type	Temperature
P3P622S01JG−08TR	ADS	8 pin, 4.4 mm TSSOP, TAPE & REEL, Green	0°C to +70°C

NOTE: A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−free

P3P622S01J

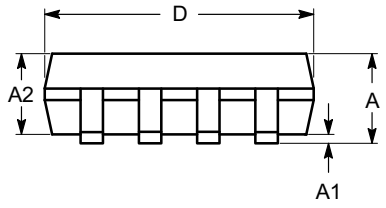
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL
ISSUE O

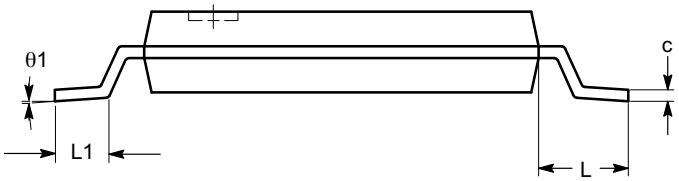


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW



END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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